Clock Control (CLK)

On Chip Oscillators

- Multiple clock sources for full flexibility in RUN/Low Power modes
  - HSE (High Speed External oscillator): 1MHz to 16MHz main osc
    → Can be bypassed with external clock
  - HSI (High Speed Internal RC): factory trimmed internal RC oscillator 16MHz calibrated in factory +/-2% max at ambient temperature
    - Feeds System clock after reset or exit from HALT/Active HALT mode for fast startup
    - Backup clock HSI/8 in case HSE failure
  - LSI (Low Speed Internal RC): 38 kHz internal RC for IWDG and optionally for the RTC/LCD and BEEP used for Auto Wake-Up (AWU) from Active HALT mode
  - LSE (Low Speed External oscillator): 32.768 kHz osc provides a precise time base with very low power consumption (max 06µA). Optionally drives the RTC/LCD for Auto Wake-Up (AWU) from Active HALT mode.
    → Can be bypassed with external clock

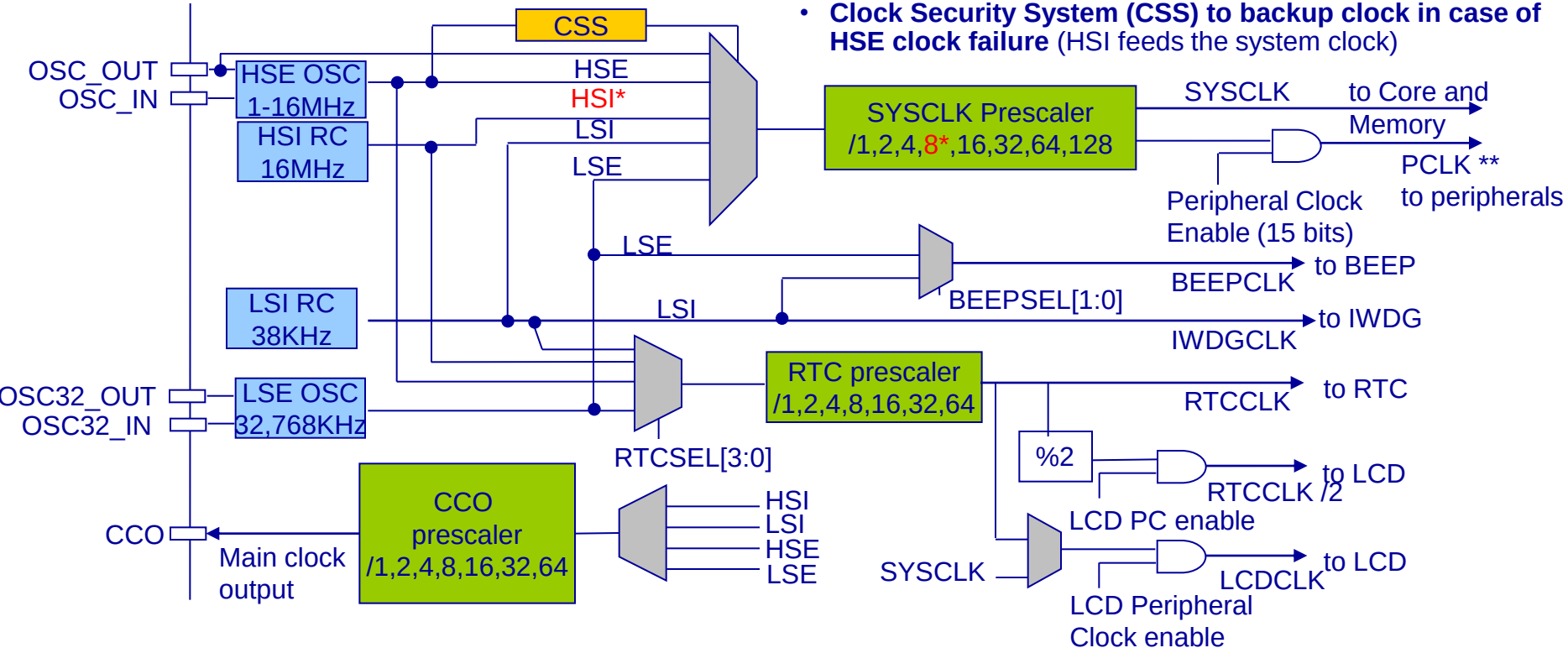
➔ ***Each clock source is enabled by Hardware when its selected to be used as source for: System clock, RTC clock, CCO output, IWDG (LSI) or BEEP (LSI/LSE) and can't be disabled while its being used.***

Clock Scheme & Features L15x

- **System clock sources**
  - HSI
  - HSE
  - LSI
  - LSE

HSI/8 default after reset*

- **Configurable dividers to provide CPU and peripherals clocks**
- **Peripheral clock gating (PCG)****
  - Enable or disable the clock for each peripherals to reduce power consumption
- **RTC/LCD Clock sources**
  - HSI
  - HSE
  - LSI
  - LSE
- **Fast and efficient System clock switching**
  - Clock sources can be changed safely on the fly in run mode through a configuration register
- **Configurable clock output on CCO Pin (PC4)**
- **Clock Security System (CSS) to backup clock in case of HSE clock failure** (HSI feeds the system clock)



(**) PCLK, clock gating for USART1,I²C1,SPI1,TIM1..4,DAC,ADC1,LCD,DMA1,WWDG,COMP

RTC and LCD clock L15x

- The RTC has two clock sources
  - **RTCCLK** used for RTC timer/counter.
    - When the HSE or HSI clock is selected as RTCCLK source, this clock must be divided to have a maximum of 1 MHz as input for the RTCCLK.
  - **SYSCLK** used for RTC register read/write access. This clock is gated by bit2 in the Peripheral clock gating register 2 (CLK_PCKENR2)

- The LCD has two clock sources
  - **RTCCLK** divided by 2 used to generate the LCD frame rate. This clock is gated by bit3 in the Peripheral clock gating register 2 (CLK_PCKENR2).
    - Consequently, even if the RTC is not used in the application the RTCCLK must be configured to drive the LCD.
  - **LCDCLK** used for LCD register read/write access. This clock is derived from SYSCLK by setting the bit3 in the Peripheral clock gating register 2 (CLK_PCKENR2).
    - In Active Halt mode the LCDCLK source is RTCCLK instead of SYSCLK.

Peripheral Clock Gating (PCG)

- PCG allows to cut the clock feeding to selected peripherals in order to decrease the power consumption. This is applicable for both Run and Wait modes

- Peripherals which clock can be gated:
  - USART1,I²C1,SPI1,TIM1..4,DAC,ADC1,LCD,DMA1,WWDG, COMP
  - RTC, LCD, BEEP (only system clock to register, not counter clock)

- After reset all peripheral clocks are disabled, to enable or disable or enable the clock for each peripheral:
  - Set/Reset the corresponding PCKENx bit in CLK_PCKENR1/2 register
  - Then set the peripheral enable bit in the corresponding control register

Configurable Clock Output (CCO)

- Steps to configure the required CCO:
  - Configure CCO pin (PC4) as output push pull (**set the related bit in CR1**)
  - Select the clock to output and the prescaler in CLK_CCOR register
- The clock source selected in the CCO register will be automatically switched ON if not done previously by the user
- In order to know if the selected clock signal is ready: check CCOSWBSY bit
- If the CCO feature is switched OFF, the CCO pin has to be re-configured in input floating (default I/O state) by the user

Clock Scheme & Features L101

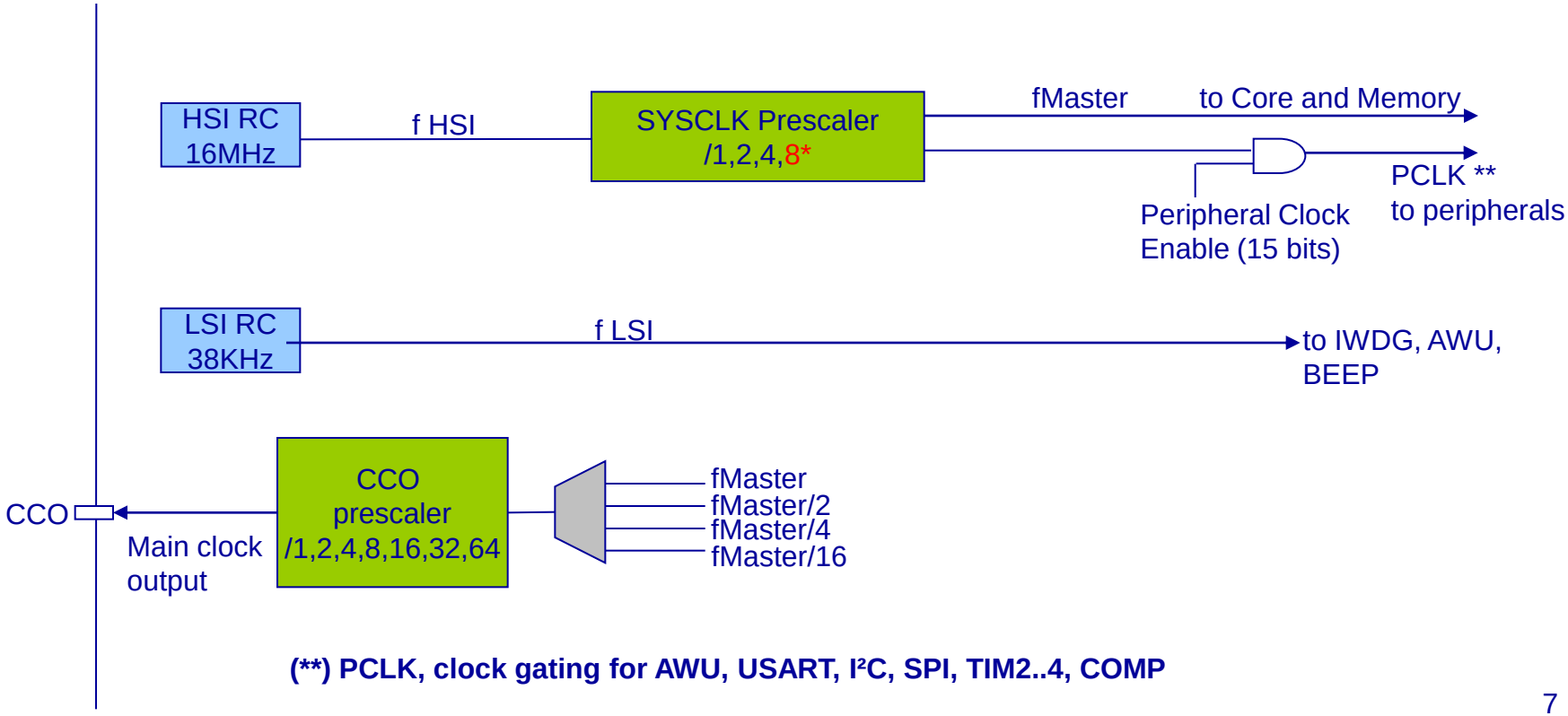
- **System clock sources**
  - HSI
  - LSI

HSI/8 default after reset*

- **Configurable dividers to provide CPU and peripherals clocks**
- **Peripheral clock gating (PCG)****
  - Enable or disable the clock for each peripherals to reduce power consumption

- **Fast and efficient System clock switching**
  - Clock sources can be changed safely on the fly in run mode through a configuration register

- **Configurable clock output on CCO Pin (PC4)**



(**) PCLK, clock gating for AWU, USART, I²C, SPI, TIM2..4, COMP

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